V-Band Low-Loss and Low-Voltage Distributed MEMS Digital Phase Shifter Using Metal-Air-Metal Capacitors

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Abstract — A low-loss digital distributed phase shifter has been developed using micromachined capacitive shunt switches for V-band communication system. Instead of conventional MIM (metal-insulator-metal) capacitors, high-Q MAM (metal-air-metal) capacitors were used in series with the MEMS shunt capacitive switches to minimize the dielectric loss. The operation voltage for the phase shifter was also reduced by applying the bias directly to the MEMS shunt switches through choke spiral inductors. The fabricated 2-bit (270°) distributed phase shifter showed low average insertion loss of 2.2 dB at 60 GHz. The return loss is better than 10 dB over a wide frequency range from 40 to 70 GHz. The circuit operates at 15-20 V bias voltages. This phase shifter is very promising for the integrated circuits at V-band requiring low loss and good return loss over a broad band.

I. INTRODUCTION

Analog phase shifters using CPW lines with distributed MEMS bridges have recently demonstrated broadband characteristics with low loss of 4.0 dB / 360° at 60 GHz [1]. However, since there was a limit on the control range of the bridge height before the bridge snaps, the analog phase shifter showed relatively small phase shift. This problem was solved by operating the MEMS bridges in the digital mode [2]-[8], where two distinct capacitance states (on : bridge snapped and off : bridge as is) were defined with a high C_{on}/C_{off} ratio. Digital phase shifters with this approach allow large phase shift and low sensitivity to electrical noise. In the published CPW digital phase shifters [2], [3], a small MIM (metal-insulator-metal) capacitor in series with the MEMS bridge capacitor was used to reduce the total shunt capacitance seen by the line, resulting in an acceptable return loss for both switching states over a wide band. Here, the biasing to the MEMS capacitor was applied through these two series capacitors, resulting in high actuation bias voltages in excess of 40 V. If this approach were to be applied at higher frequencies such as V-band, the bias voltage would be too high to be practical. This is due to the fact that the required MEMS shunt capacitance of the CPW lines decreases as frequency increases, making the switching voltage even higher. Moreover, the loss of the loaded CPW line will increase because of the low Q of the MIM capacitor at high frequencies [3]. The goal of this work was to realize a distributed CPW digital phase shifter with low loss and reasonable actuation voltage at V-band. In order to

TABLE I
Comparison of loss and pull-down voltage for several MEMS phase shifters.

Reference	Type	Average Insertion Loss	Frequency	Pull-down Volt
[1]	CPW analog Distributed type (360°)	4 dB	60 GHz	> 13 V
[2]	CPW 1-bit Distributed type (270°)	1.69 dB	35 GHz	75 V
[3]	CPW 2-bit Distributed type (270°)	4 dB	11.4 GHz	60 V
[4]	CPW 3-bit Distributed type (315°)	1.7 dB	26 GHz	60 V
[5]	Microstrip 4-bit Distributed type (337°)	3 dB	16 GHz	40-60 V
[6]	Microstrip 4-bit Resonant Line (337°)	2.25 dB	34 GHz	45 V
[7]	Microstrip 4-bit True-Time Delay (337°)	2.5 dB	10.8 GHz	70 V
[8]	Microstrip 4-bit Reflection type (337°)	1.4 dB	8 GHz	35-40 V
This work	CPW 2-bit Distributed type (270°)	2.2 dB	60 GHz	15-20 V

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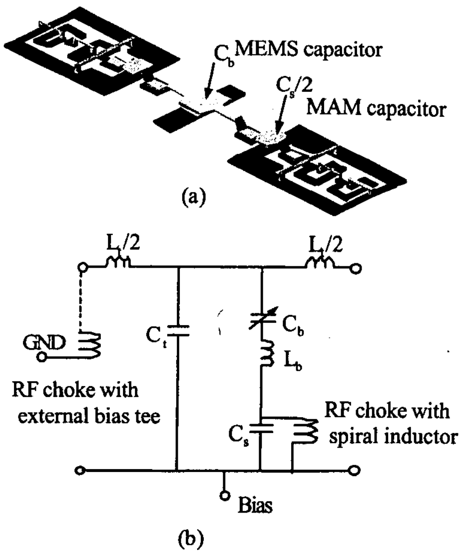


Fig. 1. (a) Schematic and (b) equivalent circuit model of the unit cell of a phase shifter with MEMS bridge and series MAM capacitors.

minimize the loss at V-band, MAM (metal-air-metal) capacitors in series with MEMS capacitor were used for the shunt capacitors. The low capacitance per unit area and high Q-factor of the MAM capacitors make MAM capacitors better suited to V-band applications than MIM capacitors. MAM structures have previously been successfully employed to demonstrate the low-loss compact filters by the authors [9]. Also, to our knowledge, Hayden will present a low-loss distributed MEMS phase shifter at Ka-band using similar MAM approach [10].

In addition to the low-loss capability made possible by the MAM capacitors, the bias voltage was also reduced in this work by employing choke spiral inductors in the bias circuit. In this way, the bias could be directly applied to the MEMS capacitors, bypassing the series MAM capacitors. The measured loss and operation voltage for several MEMS phase shifters at various bands are compared with those of this work in Table I. To the best of our knowledge, this is the first demonstration of the low-loss broadband digital MEMS phase shifters at V-band.

II. DESIGN AND FABRICATION

The 2-bit MEMS distributed phase shifter of this work consists of a high impedance CPW line (Z_0 = 96 Ω, width = 100 μm, gap = 120 μm) capacitively loaded by the periodic

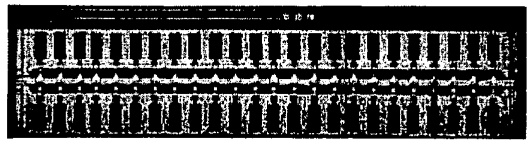


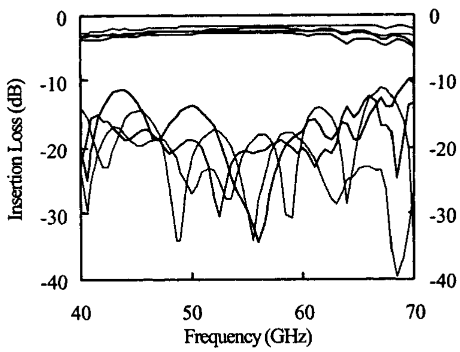
Fig. 2. Photograph of the fabricated V-band 2-bit MEMS phase shifter. Chip size is 6.3 mm x1.5 mm (24 bridges).

placement [2], [3] of a series connected MEMS bridges and MAM capacitors. The unit cell of the phase shifter is shown in Fig.1 together with the equivalent circuit model. In this design, the range of the characteristic impedances was first chosen to be from 46 to 59 Ω to guarantee good impedance matching (S_{11}, S_{22} < -13 dB) up to 75 GHz. This requires overall C_{on}/C_{off} ratio of 1.6 (40 / 25 fF) seen by the line. The length of the unit cell is 262 μm. A 262 μm-long 96 Ω line was modeled with a shunt capacitance (C_t) of 5 fF, series inductance (L_t) of 104 pH. The loaded capacitance seen by the line is the series combination of the MEMS bridge capacitance (C_b) and total MAM capacitance (C_s). The total capacitance (C_{off} or C_{on}) of the unit cell is

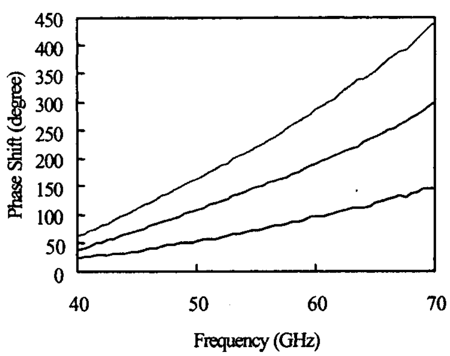
$$C_{off} = C_t + C_sC_{bu}/(C_s + C_{bu}) \text{ and}$$
$$C_{on} = C_t + C_sC_{bd}/(C_s + C_{bd}) \qquad (1)$$

where C_{bu} is MEMS bridge capacitance in the up-state position and C_{bd} in the down-state position.

Considering that the on/off capacitive ratio (C_{bd}/C_{bu}) of MEMS shunt capacitor switch with 1.5 μm air gap was about 8 in our experiment, the bridge capacitance (C_{bu}) of 69 fF (100 μm x 102 μm) in up-state and the fixed MAM capacitance ($C_s/2$) of 21 fF (62 μm x 50 μm) were determined to meet the acceptable impedance matching up to 75 GHz. The total inductance (L_b) of bridge and MAM capacitors is 26 pH. The Bragg frequencies of the unit cell in the phase shifter are over 142 GHz for both switch states. In order to achieve a very small fixed capacitance ($C_s/2$) of 21 fF, MAM capacitor was employed instead of MIM capacitor since it is less sensitive to the process variations compared with the latter. It also offers high Q-factors at high frequencies as required for V-band operation. The bias for switching is applied directly to the MEMS switch through the spiral inductors to reduce the switching DC voltage down to 15-20 V. Total inductance of two cascaded spiral inductor is 0.7 nH with self resonance frequency higher than 87 GHz. The model parameters were calculated using an electromagnetic (EM) simulator, IE3D and measured S-parameters. Simulated phase shift of the unit cell is about 11.2° at 60 GHz.



(a)



(b)

Fig. 3. Measured results of the 2-bit MEMS phase shifter. (a) Insertion loss and return loss, (b) phase shift (0°-90°-180°-270° at 60 GHz).

TABLE II
Phase shift data of the 2-bit MEMS phase shifter at 60 GHz

Phase State	**0.0°**	**90.0°**	**180.0°**	**270.0°**
Measured	**0.0°**	**97.2°**	**189.8°**	**285.2°**
Phase Error	**0.0°**	**-7.2°**	**-9.8°**	**-15.2°**

The phase shifter was fabricated with electroplated gold structures on a 520 μm-thick quartz substrate (ε_r = 3.8). The thickness of the CPW line and the bridge is 3 μm and 2 μm, respectively. A 0.3 μm-thick SiN was deposited with PECVD (plasma enhanced chemical vapor deposition) over the signal line under the bridges to avoid DC short. The details of the fabrication technology have been reported in [11].

III. MEASURENENTS

Fig.2 shows the photograph of the V-band 2-bit (90°, 180°) distributed MEMS phase shifter. The chip size is 6.3 mm x1.5 mm (24 bridges). DC bias for each one-bit phase shifter is connected to the ground pad of CPW line while the signal line is connected to DC ground through the external bias tee. When DC bias is applied, the voltage difference between the signal line and ground pad generates a strong electric field under the membrane of MEMS switch, which forces the membrane to snap down. DC block capacitors are added between the consecutive ground pads of 1-bit phase shifter sections and also between the RF probe pads and the 1-bit phase shifter sections so that the bias may be applied independently while keeping the RF ground plane continuity. The area of the DC block MIM capacitor is 80 μm x 140 μm and the thickness of SiN is 0.3 μm.

RF measurements were made on a HP 8510XF network analyzer, calibrated using LRRM (Line-Reflect-Reflect-Match) techniques with on-wafer standards. Measured results of the 2-bit phase shifter are shown in Fig. 3. As shown in Fig. 3(a), the return losses for all four switching states are better than 10 dB from 40 to 70 GHz and the average insertion loss is about 2.2 dB at 60 GHz. Fig. 3(b) illustrates the frequency-dependent phase shift for all the switching states. The average phase error for all switching states is 6.5 % at 60 GHz. Detailed phase shift data are listed in Table II.

IV. CONCLUSIONS

A V-band low-loss distributed digital MEMS phase shifter has been designed, fabricated, and tested for the first time. By direct biasing to the bridge membranes through the spiral choke inductors, the MEMS phase shifter operates at a reasonable switching voltage of 15 to 20 V. In addition, the loss of the MEMS phase shifter was reduced through the use of high-Q MAM capacitors instead of the conventional MIM capacitor. Minimization of the dielectric loss in the loaded lines resulted in low average insertion loss of 2.2 dB / 2-bit (270°) at 60 GHz.

ACKNOWLEDGEMENT

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